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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/761,253	01/16/2001	Zhenhua Wang	PHCH 000002	5183

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EXAMINER	
TRA, ANH QUAN	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 03/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/761,253	WANG, ZHENHUA	
	Examiner	Art Unit	
	Quan Tra	2816	AU

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19 and 21-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,15-18 and 21-25* is/are rejected.

7)☒ Claim(s) *10-14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 1/23/04 has been entered. The allowable subject matters of claims 2, 14, 15-17, 19 and 22-25 have been withdrawn. A new ground of rejection is introduced.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-5, 7, 15, 18, 21, 23 and 24 are rejected under 35 U.S.C. 102(b) as being anticipated by Ito et al. (USP 5744998).

As to claims 1 and 18, Ito discloses in figure 8 a voltage level monitoring circuit, comprising: a first reference current source (15a) for generating a first reference current; a second reference current source (20a) for generating a second reference current; a controllable switch (17a); a monitoring current source (13a) for generating a monitoring current derived from a voltage (VPP) to be measured; and a comparator device (16a) including a first current input (+) coupled for receiving the first reference current in response to the controllable switch being non-

conductive, and for receiving both the first reference current and second reference current in response to the controllable switch being conductive, a second current input (-) coupled for receiving the monitoring current, and at least one measuring signal output (/EN), wherein the comparator device is arranged for comparing the currents received at its two current inputs and for generating at the measuring signal output a measuring signal (/EN) with a first value (low) when the current received at its second current input is less than the current received at its first current input, and with a second value (high) when the current received at its second current input is more than the current received at its first current input.

As to claim 3, figure 8 shows a current output of the second reference current source (20a) is coupled to the comparator device (16a) through the controllable switch (17a).

As to claim 4, figure 8 shows the controllable switch (17a) is controlled by a control signal (EN) generated by the comparator device.

As to claims 5 and 21, figure 8 shows the control signal (EN) renders the controllable switch conductive when the a magnitude of the current received at the first input of the comparator device is higher than a magnitude of the current received at the second input of the comparator device, and renders the controllable switch non-conductive when the magnitude of the current received at the first input of the comparator device is lower than the magnitude of the current received at the second input of the comparator device.

As to claim 7, figure 8 shows the controllable switch (17a) includes a PMOS transistor having its source coupled the current output of the second reference current source, having its drain coupled to the first current input of the comparator device, and having its gate coupled to a control output of the comparator device.

As to claim 15, figure 8 shows the monitoring current source includes a programmable current source (the current that going through transistor 14a is varied in responsive to Vcmp. Thus, transistor 14a is a programmable current source).

As to claims 23 and 24, figure 8 shows the second reference current source and the switch are electrically connected in series in response to the switch being conductive; and the first reference current source is electrically connected in parallel to the series connection of the second reference current source and the switch in response to the switch being conductive.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-9, 15-18 and 21-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Papaliolios (USP 6259286) in view of Uya (USP 4506168).

As to claims 1, 18 and 19, Papaliolios shows in figure 1 a voltage detection circuit for detecting supply voltage Vcc. Papaliolios fails to teach the detail of the Schmitt trigger circuit. However, Uya's figure 3 shows a Schmitt trigger circuit having advantage of preventing the flow of steady state current. Therefore, it would have been obvious to one having ordinary skill in the art to use Uya's Schmitt trigger circuit for Papaliolios's Schmitt trigger circuit for the purpose of preventing the flow of steady state current. Thus, the combination of Papaliolios and Uya reference shows a voltage level monitoring circuit, comprising: a first reference current source (Uya's P1) for generating a first reference current; a second reference current source (Uya's P2)

for generating a second reference current; a controllable switch (Uya's P3); a monitoring current source (Uya's N1) for generating a monitoring current derived from a voltage (VCC or VDD) to be measured; and a comparator device (Uya's P4 and N2) including a first current input coupled for receiving the first reference current in response to the controllable switch being non-conductive, and for receiving both the first reference current and second reference current in response to the controllable switch being conductive, a second current input coupled for receiving the monitoring current, and at least one measuring signal output (Vout), wherein the comparator device is arranged for comparing the currents received at its two current inputs and for generating at the measuring signal output a measuring signal with a first value when the current received at its second current input is less than the current received at its first current input, and with a second value when the current received at its second current input is more than the current received at its first current input. As further called in for claim 19, Uya's figure 3 shows the comparator comprising first inverter (P4, N2). Uya's fails to shows a second inverter. However, it is notorious well known in the art that inverter is for inverting and buffering its input signal. Therefore, it would have been obvious to one having ordinary skill in the art to add a second inverter coupled to the output of Uya's figure inverter for the purpose of inverting and buffering the output signal Vout.

As to claim 2, Uya's figure 3 in combine with Papaliolios's figure 1 show the first reference current source includes a PMOS transistor (P1) having its source coupled for receiving the voltage (VDD or Vcc) to be measured, having its gate coupled for receiving a bias voltage (Vin), and having its drain coupled to the first current input of the comparator device.

As to claim 3, Uya's figure 3 shows a current output of the second reference current source is coupled to the comparator device through the controllable switch.

As to claim 4, Uya's figure 3 shows the controllable switch (P3) is controlled by a control signal (Vout) generated by the comparator device (10).

As to claim 5, Uya's figure 3 shows the control signal (Vout) renders the controllable switch (P3) conductive when the a magnitude of the current received at the first input of the comparator device is higher than the a magnitude of the current received at the second input of the comparator device, and renders the controllable switch non-conductive when the magnitude of the current received at the first input of the comparator device is lower than the magnitude of the current received at the second input of the comparator device.

As to claim 6, Uya's figure 3 shows the second reference current source (P2) includes a PMOS transistor having its source coupled for receiving the voltage (VDD or Vcc) to be measured, having its gate coupled for receiving a bias voltage (Vin), and having its drain coupled to the controllable switch (P3).

As to claim 7, Uya's figure 3 shows the controllable switch (P3) includes a PMOS transistor having its source coupled the current output of the second reference current source (P2), having its drain coupled to the first current input of the comparator device, and having its gate coupled to a control output (Vout) of the comparator device.

As to claim 8, the combination of Uya's figure 3 and Papaliolios's figure 1 shows the comparator device includes: a first inverter (P4, N2) having an input and an output; and a second inverter (the newly added inverter, see the rejection of claim 19 above) having an input and an output, wherein the output of the second inverter is connected to the output of the comparator

device, the input of the second inverter is coupled to the output of the first inverter, and the input of the first inverter is coupled to both the first and second current inputs of the comparator device.

As to claim 9, the combination of Uya's figure 3 and Papaliolios's figure 1 shows the output of the first inverter is coupled to the control output of the comparator device.

As to claim 15, Uya's figure 3 shows the monitoring current source includes a programmable current source (current going through N1 is varied in responsive to its input. Therefore, N1 is a programmable current source).

As to claim 16, Uya's figure 3 shows the first reference current source (P1) includes a programmable current source.

As to claim 17, Uya's figure 3 shows wherein the second reference current source (P2) includes a programmable current source.

As to claims 21 and 22, Uya's figure 3 shows the control signal (Vout) renders the controllable switch conductive when the a magnitude of the current received at the first input of the comparator device is higher than a magnitude of the current received at the second input of the comparator device, and renders the controllable switch non-conductive when the magnitude of the current received at the first input of the comparator device is lower than the magnitude of the current received at the second input of the comparator device.

As to claims 23-25, Uya's figure 3 shows the second reference current source (P2) and the switch (P3) are electrically connected in series in response to the switch (P3) being conductive; and the first reference current source (P1) is electrically connected in parallel to the

series connection of the second reference current source and the switch in response to the switch being conductive.

Allowable Subject Matter

6. Claims 10-14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 10-14 would be allowable because the prior art fails to teach or suggest the monitoring current source (4) includes: a primary current source (41) for generating a primary current (IP); a secondary current source (42) for generating the monitoring current (TM); and a process sensitive resistor (49) connected in series with said primary current source (41).

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. These references are cited as interest because they show some circuits analogous to the claimed invention.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 571-272-1755. The examiner can normally be reached on 8:00 A.M.-5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Quan Tra
Patent Examiner

March 12, 2004